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FIG. 2A is a perspective view of an exemplary embodiment of a structure for an integrated circuit having a substrate with an SDB just prior to initiation of epitaxial growth within S/D regions in accordance with the present invention;

FIG. 2B is a cross sectional view of FIG. 2A taken along the line 2B-2B;

FIG. 2C is a cross sectional view of FIG. 2A taken along the line 2C-2C;

FIG. 3 is a perspective view of the structure of FIG. 1A prior to formation of fins;

FIG. 4 is a perspective view of the structure of FIG. 3 after fins are patterned into the substrate;

FIG. 5A is a top view of an exemplary embodiment of the structure of FIG. 4 having a first dielectric fill material disposed thereon;

FIG. 5B is a cross sectional view of FIG. 5A taken along the line 5B-5B;

FIG. 5C is a cross sectional view of FIG. 5A taken along the line 5C-5C;

FIG. 5D is a cross sectional view of FIG. 5A taken along the line 5D-5D;

FIG. 6A is a top view of an exemplary embodiment of the structure of FIG. 5A having a photo resist layer disposed over the entirety of the first dielectric fill material;

FIG. 6B is a cross sectional view of FIG. 6A taken along the line 6B-6B;

FIG. 6C is a cross sectional view of FIG. 6A taken along the line 6C-6C;

FIG. 6D is a cross sectional view of FIG. 6A taken along the line 6D-6D;

FIG. 7A is a top view of an exemplary embodiment of the structure of FIG. 6A after an isolation region has been anisotropically etched into the structure;

FIG. 7B is a cross sectional view of FIG. 7A taken along the line 7B-7B;

FIG. 7C is a cross sectional view of FIG. 7A taken along the line 7C-7C;

FIG. 7D is a cross sectional view of FIG. 7A taken along the line 7D-7D;

FIG. 8A is a top view of an exemplary embodiment of the structure of FIG. 7A after self-aligned resist edges of a resist strip have been trimmed;

FIG. 8B is a cross sectional view of FIG. 8A taken along the line 8B-8B;

FIG. 8C is a cross sectional view of FIG. 8A taken along the line 8C-8C;

FIG. 8D is a cross sectional view of FIG. 8A taken along the line 8D-8D;

FIG. 9A is a top view of an exemplary embodiment of the structure of FIG. 8A after exposed end portions of a fin hardmask have been removed;

FIG. 9B is a cross sectional view of FIG. 9A taken along the line 9B-9B;

FIG. 9C is a cross sectional view of FIG. 9A taken along the line 9C-9C;

FIG. 9D is a cross sectional view of FIG. 9A taken along the line 9D-9D;

FIG. 10A is a top view of an exemplary embodiment of the structure of FIG. 9A after a remaining photoresist layer has been removed;

FIG. 10B is a cross sectional view of FIG. 10A taken along the line 10B-10B;

FIG. 10C is a cross sectional view of FIG. 10A taken along the line 10C-10C;

FIG. 10D is a cross sectional view of FIG. 10A taken along the line 10D-10D;

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FIG. 11A is a top view of an exemplary embodiment of the structure of FIG. 10A after a second dielectric fill material has been disposed over the structure;

FIG. 11B is a cross sectional view of FIG. 11A taken along the line 11B-11B;

FIG. 11C is a cross sectional view of FIG. 11A taken along the line 11C-11C;

FIG. 11D is a cross sectional view of FIG. 11A taken along the line 11D-11D;

FIG. 12A is a top view of an exemplary embodiment of the structure of FIG. 11A after the first dielectric fill material has been recessed;

FIG. 12B is a cross sectional view of FIG. 10A taken along the line 12B-12B;

FIG. 12C is a cross sectional view of FIG. 12A taken along the line 12C-12C;

FIG. 12D is a cross sectional view of FIG. 12A taken along the line 12D-12D;

FIG. 13A is a top view of an exemplary embodiment of the structure of FIG. 12A after the remaining fin hardmask has been removed;

FIG. 13B is a cross sectional view of FIG. 13A taken along the line 13B-13B;

FIG. 13C is a cross sectional view of FIG. 13A taken along the line 13C-13C;

FIG. 13D is a cross sectional view of FIG. 13A taken along the line 13D-13D;

FIG. 14A is a top view of an exemplary embodiment of the structure of FIG. 13A after a dummy gate and active gates have been disposed thereon;

FIG. 14B is a cross sectional view of FIG. 14A taken along the line 14B-14B;

FIG. 14C is a cross sectional view of FIG. 14A taken along the line 14C-14C; and

FIG. 14D is a cross sectional view of FIG. 14A taken along the line 14D-14D.

DETAILED DESCRIPTION

Certain exemplary embodiments will now be described to provide an overall understanding of the principles of the structure, function, manufacture, and use of the methods, systems, and devices disclosed herein. One or more examples of these embodiments are illustrated in the accompanying drawings. Those skilled in the art will understand that the methods, systems, and devices specifically described herein and illustrated in the accompanying drawings are non-limiting exemplary embodiments and that the scope of the present invention is defined solely by the claims. The features illustrated or described in connection with one exemplary embodiment may be combined with the features of other embodiments. Such modifications and variations are intended to be included within the scope of the present invention.

Referring to FIGS. 1A, 1B and 1C, an exemplary embodiment of a structure 10 for an integrated circuit formed utilizing FinFET technology and having a prior art single diffusion break (SDB) 12 is presented. FIG. 1A is a perspective view of structure 10 at an intermediate stage of its manufacturing process, just prior to initiation of epitaxial growth within source/drain (S/D) regions 14 and 16. FIG. 1B is a cross sectional view of FIG. 1A taken along the line 1B-1B, which cuts through fins 26 and 36. FIG. 1C is a cross sectional view of FIG. 1A taken along the line 1C-1C, which cuts a region between the parallel rows of fins.

Structure 10 includes a pair of opposing active Rx regions 18 and 20, which are separated by an isolation region 22. In